REMARKS

Reconsideration and allowance are respectfully requested in view of the following remarks.

Claims 1-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dye in view of Yano. Applicants have amended claim 1 to recite "a special purpose reconfigurable control unit operable to control which rows of the array of reconfigurable data-path oriented cells are activated, each row representing a stage of a customized pipeline, the special purpose reconfigurable control unit controlling activation of the rows in a dataflow fashion." There is no teaching or suggestion for the claimed control unit in the Dye or Yano references. For example, the Examiner has previously pointed to the Yano control logic. However, Yano teaches that the control logic is "a reprogramming control portion 17 for reprogramming the circuit composed of the FPGA 19 upon receipt of output of the diagnosis portion 16" (col. 6, lines 23-25). Thus, the Yano control logic is limited in use for reprogramming of the FPGA (this is equivalent to the configuration control unit 13 described in the specification and shown in Figure 4 of the application). In the claimed invention, however, the control logic at issue functions to control "which rows of the array of reconfigurable data-path oriented cells are activated, each row representing a stage of a customized pipeline, the special purpose reconfigurable control unit controlling activation of the rows in a dataflow fashion." This operation is neither disclosed nor suggested by Yano. In view of the foregoing, Applicants respectfully submit that claim 1, along with its dependent claims, is patentable over the art of record.

An advantage of the claimed invention over the art is that a user does not need to directly describe, for example using hardware description language, how the different pipeline stages are activated during run time. This is instead handled by the claimed special purpose reconfigurable control unit. A user can thus program the claimed architecture using high level languages (see, specification page 12). Another advantage is that the control unit can operate more efficiently (with a fixed high working frequency). Yet another advantage is that because the control unit activates only the needed rows there is a reduction in power consumption by the circuit. Advantages were described in the specification at pages 11-12.

With respect to claim 9, Applicants claim that the "control unit is a hardwired, run-time programmable Data-Flow-Graph based control unit synchronizing the pipelined computation of the gate-array cells." The claimed hardwired control unit differs from the cited prior art wherein execution control is mapped together with the data-path in the cells of the array. An advantage of the hardwired control unit as claimed is that it works independently from the performed function in the data-path. There also is no teaching for the Data-Flow-Graph based control operation in connection with the synchronizing operation.

In new claim 26, Applicants claim that the "control unit is further operable to control synchronization of the array of reconfigurable data-path oriented cells and the processor." There is no teaching or suggestion in Yano for the control logic operating to perform the cited synchronization operation. Claim 26 is accordingly submitted to define over the cited prior art.

Applicants recite in new claim 28 the use of a data flow model in connection with control unit operation to calculate for each cycle which row of the pipeline stage is to perform

computations. This feature of data flow model driven operation with respect to control unit operation on the pipeline state of cells is neither disclosed nor suggested by the prior art.

In new claim 33, Applicants claim register locking. While this locking concept by itself may be taught by the prior art, there is no teaching or suggestion in the prior art for the combined use of register locking and the control unit as claimed.

In claim 36, Applicants claim organizing the array in regions composed of a configurable number of rows of cells. This structure is not taught or suggested by the prior art. Additionally, Applicants claim a separation with respect to region operation in that when one region is being reprogrammed the other regions remain in execution. These features are not disclosed by the prior art.

New claim 38 is patentable over the cited prior art because there is no teaching or suggestion for the claimed combination of an array of reconfigurable data-path oriented cells, a configuration control unit, and an operation control unit.

In view of the above, it is believed that this application is in condition for allowance, and such a Notice is respectfully requested.

Respectfully submitted,

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